AF/GP2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#46 Appeal Brief 7300

In re the Application of:

KIRA, et al.

Serial Number: 08/897,953

Filed: July 24, 1997

Group Art Unit: 2814

Examiner: D. Graybill

For: METHOD AND SYSTEM FOR FABRICATING SEMICONDUCTOR DEVICE

SUBMISSION OF APPEAL BRIEF

Director of Patents and Trademarks
Washington, D.C. 20231

July 31, 2000

Sir:

Submitted herewith are an original and two copies of an Appeal Brief in the above-identified U.S. patent application.

Please charge the amount of $300.00 to cover the cost for the Appeal Brief to our Deposit Account No. 01-2340.

If any additional fees are due in connection with this submission, please charge our Deposit Account No. 01-2340. This paper is filed in triplicate.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON

William L. Brooks
Attorney for Applicants
Registration No. 34,129

Attorney Docket No. 950107A
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel: (202) 659-2930
WLB:mlg

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Sir:

This is an appeal from the Office Action dated November 30, 2000 in which claims 3-6, 8 and 11-17 were finally rejected.

A Notice of Appeal and a Petition for Extension of Time were timely filed on May 30, 2000.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Fujitsu Limited
1015, Kamikodanaka, Nakahara-ku
Kawasaki-shi, Kanagawa, 211, JAPAN

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 3, 5-6, 8 and 15-17 on appeal have been finally rejected as follows:

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ARMSTRONG, WESTERMAN, HATTORI,
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1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel (202) 659-2930
Fax (202) 887-0357

Date: July 31, 2000
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1. Claims 3, 5-6, 8 and 15 have been finally rejected under 35 USC §103(a) as unpatentable over Appellants' Admitted Prior Art (hereinafter "**APA**") in view of JP 58180091 to Maeda (hereinafter "**Maeda**") and JP 4302444 to Koga (hereinafter "**Koga**").

2. Claims 12 and 16 have been finally rejected under 35 USC §103(a) as unpatentable over the combination of **APA**, **Maeda**, **Koga** and further in combination with U.S. Patent 5,548,091 to DiStefano (hereinafter "**DiStefano**"); and

3. Claim 17 has been finally rejected under 35 USC §103(a) as unpatentable over the combination of **APA**, **Maeda**, **Koga** and further in combination with U.S. Patent 5,115,545 to Fujimoto et al. ("**Fujimoto et al.**").

IV. STATUS OF AMENDMENTS

All amendments have been entered, including the Amendment After Final Rejection filed May 1, 2000, in which claims 4 and 11-14 were canceled and claims 5 and 6 were amended. Thus, claims 4 and 11-14 are not under consideration in this appeal, contrary to the erroneous indication by the Examiner in the Advisory Action that they are.

V. CLAIMS ON APPEAL

A clean copy of claims 3, 5-6, 8 and 15-17 on appeal is attached hereto as Exhibit A.

VI. SUMMARY OF THE INVENTION

The present invention generally relates to a fabrication method of a semiconductor device comprising the steps of: (a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips (specification, page 7, line 28 - page 8, line 11; Fig. 3, step S1); (b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate (specification, page 8, lines 23-34; Fig. 3, step S4); (c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means (Fig. 3, step S5) and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed (specification, page 8, line 35 - page 9, line 18; Fig. 3, step S6); (d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive (specification, page 9, lines 19-23; Fig. 3, step S7); and (e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips (specification, page 9, line 23 - page 10, line 13; Fig. 3, step S8).

VII. THE ISSUES

1. Whether the invention, as recited in Appellants' claims 3, 5-6, 8 and 15 on appeal are unpatentable under 35 USC §103(a) over **APA** in view of **Maeda** and **Koga**.

2. Whether the invention, as recited in Appellants' claims 12 and 16 on appeal, are unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **DiStefano**; and

3. Whether the invention, as recited in Appellants' claim 17 on appeal, is unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **Fujimoto et al**.

VIII. GROUPING OF THE CLAIMS

Rejected claims 3, 5-6, 8 and 15-17 on appeal should stand or fall together, because claims 3, 5-6, 8 and 16-17 depend from independent claim 15.

IX. ARGUMENT WITH RESPECT TO THE ISSUES

A. THE REFERENCES

The Examiner has relied upon four (4) prior art references in the 35 USC §103(a) rejections of the claims, namely, **Maeda**, **Koga**, **DiStefano** and **Fujimoto et al**.

Maeda discloses a method of adhering leadless electrical parts in which the adhesive is heated prior to mounting of the leadless electrical parts in order to increase the viscosity of the adhesive. Then, after mounting of the leadless electrical parts on the adhesive, heat or radioactive rays are applied to the printed wiring board. Pg. 7, lines 7-21 disclose that the first heating process "is carried out from an upper place by a far-infrared-rays heater 4", as shown in Fig. 2(b).

Furthermore, pg. 7, lines 22-31 disclose that the second heating process is carried out by applying ultraviolet rays for 15 seconds by a high-pressure mercury lamp having a reflecting plate 7. Line 30 specifically refers to this heating as a "radiating process".

Kogo discloses a mounting method for a semiconductor on a substrate in which after the plurality of semiconductor elements have been bonded temporarily on the substrate via the anisotropically conductive film, the plurality of semiconductor elements are heated and pressurized collectively.

DiStefano discloses a method of mounting connection components on semiconductor chips. The method includes the step of aligning the connection component with the chip so that the leads on the connection component are aligned with contacts on the chip and bonding the bottom surface of the support structure to a surface of the chip by engaging the bottom surface of the support structure against the chip surface and activating the adhesive on the support structure bottom surface while marinating the alignment between the conductors of the connection component and the contacts on the chip. most preferably, the bonding step includes the step of moving the connection component relative to the chip in an engagement direction substantially normal to the surface of the chip after the aligning step so as to engage the bottom surface of the connection component with the surface of the chip. Such normal motion can be readily combined with an alignment process using automatic pattern recognition with other automated alignment steps without disturbing the alignment achieved by these steps.

The bonding step desirably includes the step of momentarily heating the adhesive while the adhesive is engaged between the bottom surface of the connection component and the surface of th chip. In a particularly preferred arrangement, the chip may be at an elevated temperature prior to

the bonding step, so that the adhesive is heated by heat transferred from the chip to the adhesive when the adhesive is engaged with the chip surface. The adhesive desirably is solid and non-tacky prior to engagement with the hot chip.

Fujimoto discloses an apparatus for connecting a semiconductor device having multi-electrodes at small pitches to a wiring board in such a manner so as to secure the alignment between the electrodes and he wiring patterns, the chips being secured to the wiring board with an insulating resin of a photo-setting nature. The apparatus eliminates the necessity of using heat or supersonic waves, thereby reducing equipment costs.

B. SUMMARY OF EXAMINER'S REJECTIONS

1. Claims 3, 5-6, 8 and 15 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over th combination of **APA** and **Maeda** and further in combination with **Koga**.

The Examiner urges that Appellants teach as conventional a process comprising the steps of forming leveled projection electrode studs 14 on a semiconductor chip 11 by wire-bonding; forming conductive adhesive 16a on the electrodes by a conductive adhesive 16 that has been skidded on a plate 15a and then transcribed onto the electrodes; applying a thermosetting insulating adhesive 18 to areas of mounting parts where the chip is to be mounted on a substrate 17; aligning the chip to the mounting parts at a first stage and performing a first fixing of the chips with a first pressure by a bonding head to which the chip is absorbed; and, thereafter, heating the substrate on which the chip is fixed with a thermosetting temperature of the adhesive. See page 1, line 23 to page 2, line 22 of the specification of the application on appeal.

The Examiner asserts, however, that Appellants do not appear to explicitly teach as conventional a process comprising a plurality of chips, and the steps of heating the adhesive on the substrate with a half-thermosetting temperature os as to harden the adhesive on the substrate to a half-thermosetting state by heating means; moving the substrate to a second stage, while the chips on the substrate are held at their position by the half-thermosetting state of the adhesive; thereafter, heating at the second stage the substrate on which the chips are fixed. The Examiner cited **Maeda** for teaching this process at page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full paragraph. Moreover, the Examiner urges that it would have been obvious to combine the process of **Maeda** with the process of **APA** because it would enable accurate alignment of plural chips before the final fixing step of the conventional art.

The Examiner urges that the combination of **APA** and **Maeda** does not appear to explicitly teach a process comprising wherein a second fixing is simultaneously performed for each of the chips with a second pressure, and wherein in the heating step (e) while heating the adhesive on the mounting parts a pressure is applied to the chips. Nevertheless, the Examiner cited **Kogo** for teaching a process comprising wherein a second fixing is simultaneously performed for each of plural chips with second pressure, and wherein in a heating step while heating an adhesive on mounting parts a pressure is applied to the chips. The Examiner concludes that it would have been obvious to combine the process of **Koga** with the process of the applied prior art because it would facilitate bonding.

The Examiner admits that the combination of applied prior art does not appear to explicitly teach a process wherein the second pressure is greater than the first pressure, but urges that it would

have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure limitation, and urges that it appears *prima facie* that the process would possess utility using another relative pressure. The Examiner notes that it has been held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

2. Claims 12 and 16 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga**, as applied to claims 3, 5-6, 8 and 15, and further in combination with **DiStefano**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising wherein in the heating step (c) heating the adhesive is performed by a heat plate on which the substrate is placed. Regardless, the Examiner urges that, at column 9, lines 3-63 **DiStefano** teaches a process comprising wherein in a heating step heating the adhesive is performed by a heat plate 58 on which a substrate mounting chips is placed. The Examiner urges that it would have been obvious to combine the process of **DiStefano** with the process of the applied prior art because it would facilitate adhesive curing.

3. Claim 17 on appeal was finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga** as applied to claims 3, 5-6, 8 and 15 supra, and further in combination with **Fujimoto**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate. The

Examiner cites **Koga** for teaching a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is provided on the heat block corresponding to the mounting parts of the substrate. The Examiner cites **Fujimoto** for teaching a single bonding head 52 for each chip. The Examiner urges that it would have been obvious to combine the process of **Fujimoto** and the process of **Koga** by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. The Examiner urges that it would have been obvious to combine the heat block of the combination of **Fujimoto** and **Koga** with **APA** because it would facilitate bonding.

C. APPELLANTS' ARGUMENT

1. APA, IN COMBINATION WITH MAEDA AND KOGA, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 3, 5-6, 8 AND 15 ON APPEAL.

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that the structural elements by combined in a similar manner as the claimed invention. See, e.g., *Panduit*

Corp. v. Dennison Mfg. Co., 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), vacated on other grounds, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

Maeda discloses a method of adhering leadless electrical parts in which the adhesive is heated prior to mounting of the leadless electrical parts in order to increase the viscosity of the adhesive. Then, after mounting of the leadless electrical parts on the adhesive, heat or radioactive rays are applied to the printed wiring board. Pg. 7, lines 7-21 disclose that the first heating process "is carried out from an upper place by a far-infrared-rays heater 4", as shown in Fig. 2(b). Furthermore, pg. 7, lines 22-31 disclose that the second heating process is carried out by applying ultraviolet rays for 15 seconds by a high-pressure mercury lamp having a reflecting plate 7. Line 30 specifically refers to this heating as a "radiating process".

Summarizing, **Maeda** teaches the step of heating an insulating adhesive to increase the viscosity thereof so as to prevent electrical parts from moving. However, **Maeda** fails to teach or suggest that the electrical parts are held with pressure, as recited in the claims on appeal.

The Examiner has urged, however, that application of such pressure would be inherent in **Maeda** because **Maeda** teaches the use of a bonding head to mount the chips into the adhesive. Column 3, lines 3-5 disclose "loading the electronic parts on the printed circuit substrate and pressing them on the adhesive."

Maeda fails to teach, mention or suggest a second pressure application of pressure on the chips which is greater than the first application of pressure, as recited in the claims on appeal.

The Examiner has applied **Koga** for teaching two separate application steps, as noted in the Abstract of **Koga**:

> ... Then, since the surface of the anisotropically conductive film 7 is provided with adhesive power, the semiconductor element 1 is bonded temporarily to a substrate 5. The substrate 5 which has finished its temporarily bonding process is conveyed to a bonding sage 11 by using a substrate conveyance device 12: it is position (sic). A bonding head 25 is driven downward in a state that the temperature at its lower-end part is kept at 190°C; it presses many semiconductor elements (sic), ... in the direction of the substrate 5 at a definite pressure.

Koga fails to explicitly teach, however, that the second pressure is greater than the first pressure, as recited in the claims on appeal, as the Examiner has admitted. The Examiner has urged, however, that this would be an obvious choice ascertainable by routine experimentation. The Examiner has held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a "particular unobvious purpose, produce an unexpected result, or otherwise critical."

Appellants respectfully disagree and submit that such a claimed relation between the first and second pressure would require undue experimentation to produce. **Koga** fails to provide any reason why such relationship would be important.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

2. APA, IN COMBINATION WITH MAEDA, KOGA AND DISTEFANO, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 12 AND 16 ON APPEAL.

DiStefano has been cited for teaching a heating step performed by a heat plate 58 on which a substrate is placed.

DiStefano is not combinable with **Maeda** to teach the present invention because, while **DiStefano** discloses conductive heating, which requires pressure, **Maeda** specifically discloses radiative heating without pressure.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

3. APA, IN COMBINATION WITH MAEDA, KOGA AND FUJIMOTO ET AL., FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIM 17.

Fujimoto et al. has been cited for teaching a single bonding head 52 for each chip "without the need for using heat or supersonic waves" (see Abstract of **Fujimoto et al.**"), which teaches away from the two heating steps recited in claim 15 on appeal, from which claim 17 on appeal depends.

DiStefano and **Fujimoto et al.** both fail to teach, mention, or suggest the two-step heating with pressure applied to the semiconductor chips as recited in claim 15 on appeal and none of the cited references teaches, mentions, or suggests the relationship between the pressure applied in the two heating steps, as recited in claim 15 on appeal.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

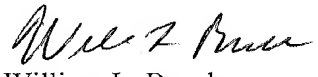
X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's 35 USC §103(a) rejections of claims 3, 5-6, 8 and 15-17 on appeal and to instruct the Examiner to pass this application to issue.

In the event this paper is not timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI
McLELAND & NAUGHTON



William L. Brooks
Attorney for Applicants
Registration No. 34,129

Attorney Docket No. 950107A
1725 K Street, N.W.
Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
WLB:mlg
Enclosure: Appendix A containing Claims on Appeal

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Filed: July 24, 1997 Examiner: D. Graybill

For: METHOD AND SYSTEM FOR FABRICATING SEMICONDUCTOR DEVICE

CLAIMS ON APPEAL

Director of Patents and Trademarks
Washington, D.C. 20231 July 31, 2000

Sir:

The claims on appeal are 3, 5-6, 8 and 15-17, presented below.

3. The fabrication method of the semiconductor device as claimed in claim 15, wherein said fixing is simultaneously performed for each of said semiconductor chips with said second pressure.

5. The fabrication method of the semiconductor device as claimed in claim 15, wherein said plurality of the projection electrodes are formed as studs by wire-bonding, the studs being leveled.

6. The fabrication method of the semiconductor device as claimed in claim 15, wherein said step (a) further comprises the steps of (a-1) forming a conductive adhesive on said projection electrodes.

8. The fabrication method of the semiconductor device as claimed in claim 6, wherein in the step (a-1), said conductive adhesive on the projection electrodes is formed by a conductive adhesive, that has been skidded on a plate, and then transcribed onto the projection electrodes.

15. A fabrication method of a semiconductor device comprising the steps of:

(a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;

(b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;

(c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed;

(d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and

(e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

16. A fabricating method according to claim 15, wherein in the heating step (c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate is placed.

17. A fabrication method according to claim 15, wherein in the heating step (e), heating the thermosetting insulating adhesive is performed by a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.

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ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON
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VI. SUMMARY OF THE INVENTION

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VII. THE ISSUES

1. Whether the invention, as recited in Appellants' claims 3, 5-6, 8 and 15 on appeal are unpatentable under 35 USC §103(a) over **APA** in view of **Maeda** and **Koga**.

2. Whether the invention, as recited in Appellants' claims 12 and 16 on appeal, are unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **DiStefano**; and

3. Whether the invention, as recited in Appellants' claim 17 on appeal, is unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **Fujimoto et al**.

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DiStefano discloses a method of mounting connection components on semiconductor chips. The method includes the step of aligning the connection component with the chip so that the leads on the connection component are aligned with contacts on the chip and bonding the bottom surface of the support structure to a surface of the chip by engaging the bottom surface of the support structure against the chip surface and activating the adhesive on the support structure bottom surface while marinating the alignment between the conductors of the connection component and the contacts on the chip. most preferably, the bonding step includes the step of moving the connection component relative to the chip in an engagement direction substantially normal to the surface of the chip after the aligning step so as to engage the bottom surface of the connection component with the surface of the chip. Such normal motion can be readily combined with an alignment process using automatic pattern recognition with other automated alignment steps without disturbing the alignment achieved by these steps.

The bonding step desirably includes the step of momentarily heating the adhesive while the adhesive is engaged between the bottom surface of the connection component and the surface of th chip. In a particularly preferred arrangement, the chip may be at an elevated temperature prior to

the bonding step, so that the adhesive is heated by heat transferred from the chip to the adhesive when the adhesive is engaged with the chip surface. The adhesive desirably is solid and non-tacky prior to engagement with the hot chip.

Fujimoto discloses an apparatus for connecting a semiconductor device having multi-electrodes at small pitches to a wiring board in such a manner so as to secure the alignment between the electrodes and he wiring patterns, the chips being secured to the wiring board with an insulating resin of a photo-setting nature. The apparatus eliminates the necessity of using heat or supersonic waves, thereby reducing equipment costs.

B. SUMMARY OF EXAMINER'S REJECTIONS

1. Claims 3, 5-6, 8 and 15 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over th combination of **APA** and **Maeda** and further in combination with **Koga**.

The Examiner urges that Appellants teach as conventional a process comprising the steps of forming leveled projection electrode studs 14 on a semiconductor chip 11 by wire-bonding; forming conductive adhesive 16a on the electrodes by a conductive adhesive 16 that has been skidded on a plate 15a and then transcribed onto the electrodes; applying a thermosetting insulating adhesive 18 to areas of mounting parts where the chip is to be mounted on a substrate 17; aligning the chip to the mounting parts at a first stage and performing a first fixing of the chips with a first pressure by a bonding head to which the chip is absorbed; and, thereafter, heating the substrate on which the chip is fixed with a thermosetting temperature of the adhesive. See page 1, line 23 to page 2, line 22 of the specification of the application on appeal.

The Examiner asserts, however, that Appellants do not appear to explicitly teach as conventional a process comprising a plurality of chips, and the steps of heating the adhesive on the substrate with a half-thermosetting temperature os as to harden the adhesive on the substrate to a half-thermosetting state by heating means; moving the substrate to a second stage, while the chips on the substrate are held at their position by the half-thermosetting state of the adhesive; thereafter, heating at the second stage the substrate on which the chips are fixed. The Examiner cited **Maeda** for teaching this process at page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full paragraph. Moreover, the Examiner urges that it would have been obvious to combine the process of **Maeda** with the process of **APA** because it would enable accurate alignment of plural chips before the final fixing step of the conventional art.

The Examiner urges that the combination of **APA** and **Maeda** does not appear to explicitly teach a process comprising wherein a second fixing is simultaneously performed for each of the chips with a second pressure, and wherein in the heating step (e) while heating the adhesive on the mounting parts a pressure is applied to the chips. Nevertheless, the Examiner cited **Kogo** for teaching a process comprising wherein a second fixing is simultaneously performed for each of plural chips with second pressure, and wherein in a heating step while heating an adhesive on mounting parts a pressure is applied to the chips. The Examiner concludes that it would have been obvious to combine the process of **Koga** with the process of the applied prior art because it would facilitate bonding.

The Examiner admits that the combination of applied prior art does not appear to explicitly teach a process wherein the second pressure is greater than the first pressure, but urges that it would

have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure limitation, and urges that it appears *prima facie* that the process would possess utility using another relative pressure. The Examiner notes that it has been held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

2. Claims 12 and 16 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga**, as applied to claims 3, 5-6, 8 and 15, and further in combination with **DiStefano**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising wherein in the heating step (c) heating the adhesive is performed by a heat plate on which the substrate is placed. Regardless, the Examiner urges that, at column 9, lines 3-63 **DiStefano** teaches a process comprising wherein in a heating step heating the adhesive is performed by a heat plate 58 on which a substrate mounting chips is placed. The Examiner urges that it would have been obvious to combine the process of **DiStefano** with the process of the applied prior art because it would facilitate adhesive curing.

3. Claim 17 on appeal was finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga** as applied to claims 3, 5-6, 8 and 15 supra, and further in combination with **Fujimoto**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate. The

Examiner cites **Koga** for teaching a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is provided on the heat block corresponding to the mounting parts of the substrate. The Examiner cites **Fujimoto** for teaching a single bonding head 52 for each chip. The Examiner urges that it would have been obvious to combine the process of **Fujimoto** and the process of **Koga** by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. The Examiner urges that it would have been obvious to combine the heat block of the combination of **Fujimoto** and **Koga** with **APA** because it would facilitate bonding.

C. APPELLANTS' ARGUMENT

1. APA, IN COMBINATION WITH MAEDA AND KOGA, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 3, 5-6, 8 AND 15 ON APPEAL.

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that the structural elements by combined in a similar manner as the claimed invention. See, e.g., *Panduit*

Corp. v. Dennison Mfg. Co., 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), vacated on other grounds, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

Maeda discloses a method of adhering leadless electrical parts in which the adhesive is heated prior to mounting of the leadless electrical parts in order to increase the viscosity of the adhesive. Then, after mounting of the leadless electrical parts on the adhesive, heat or radioactive rays are applied to the printed wiring board. Pg. 7, lines 7-21 disclose that the first heating process "is carried out from an upper place by a far-infrared-rays heater 4", as shown in Fig. 2(b). Furthermore, pg. 7, lines 22-31 disclose that the second heating process is carried out by applying ultraviolet rays for 15 seconds by a high-pressure mercury lamp having a reflecting plate 7. Line 30 specifically refers to this heating as a "radiating process".

Summarizing, **Maeda** teaches the step of heating an insulating adhesive to increase the viscosity thereof so as to prevent electrical parts from moving. However, **Maeda** fails to teach or suggest that the electrical parts are held with pressure, as recited in the claims on appeal.

The Examiner has urged, however, that application of such pressure would be inherent in **Maeda** because **Maeda** teaches the use of a bonding head to mount the chips into the adhesive. Column 3, lines 3-5 disclose "loading the electronic parts on the printed circuit substrate and pressing them on the adhesive."

Maeda fails to teach, mention or suggest a second pressure application of pressure on the chips which is greater than the first application of pressure, as recited in the claims on appeal.

The Examiner has applied **Koga** for teaching two separate application steps, as noted in the Abstract of **Koga**:

> ... Then, since the surface of the anisotropically conductive film 7 is provided with adhesive power, the semiconductor element 1 is bonded temporarily to a substrate 5. The substrate 5 which has finished its temporarily bonding process is conveyed to a bonding sage 11 by using a substrate conveyance device 12: it is position (sic). A bonding head 25 is driven downward in a state that the temperature at its lower-end part is kept at 190°C; it presses many semiconductor elements (sic), ... in the direction of the substrate 5 at a definite pressure.

Koga fails to explicitly teach, however, that the second pressure is greater than the first pressure, as recited in the claims on appeal, as the Examiner has admitted. The Examiner has urged, however, that this would be an obvious choice ascertainable by routine experimentation. The Examiner has held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a "particular unobvious purpose, produce an unexpected result, or otherwise critical."

Appellants respectfully disagree and submit that such a claimed relation between the first and second pressure would require undue experimentation to produce. **Koga** fails to provide any reason why such relationship would be important.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

2. APA, IN COMBINATION WITH MAEDA, KOGA AND DISTEFANO, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 12 AND 16 ON APPEAL.

DiStefano has been cited for teaching a heating step performed by a heat plate 58 on which a substrate is placed.

DiStefano is not combinable with **Maeda** to teach the present invention because, while **DiStefano** discloses conductive heating, which requires pressure, **Maeda** specifically discloses radiative heating without pressure.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

3. APA, IN COMBINATION WITH MAEDA, KOGA AND FUJIMOTO ET AL., FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIM 17.

Fujimoto et al. has been cited for teaching a single bonding head 52 for each chip "without the need for using heat or supersonic waves" (see Abstract of **Fujimoto et al.**"), which teaches away from the two heating steps recited in claim 15 on appeal, from which claim 17 on appeal depends.

DiStefano and **Fujimoto et al.** both fail to teach, mention, or suggest the two-step heating with pressure applied to the semiconductor chips as recited in claim 15 on appeal and none of the cited references teaches, mentions, or suggests the relationship between the pressure applied in the two heating steps, as recited in claim 15 on appeal.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's 35 USC §103(a) rejections of claims 3, 5-6, 8 and 15-17 on appeal and to instruct the Examiner to pass this application to issue.

In the event this paper is not timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI
McLELAND & NAUGHTON

William L. Brooks
Attorney for Applicants
Registration No. 34,129

Attorney Docket No. 950107A
1725 K Street, N.W.
Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
WLB:mlg
Enclosure: Appendix A containing Claims on Appeal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:

KIRA, et al.

Serial Number: 08/897,953 Group Art Unit: 2814

Filed: July 24, 1997 Examiner: D. Graybill

For: METHOD AND SYSTEM FOR FABRICATING SEMICONDUCTOR DEVICE

CLAIMS ON APPEAL

Director of Patents and Trademarks
Washington, D.C. 20231 July 31, 2000

Sir:

The claims on appeal are 3, 5-6, 8 and 15-17, presented below.

3. The fabrication method of the semiconductor device as claimed in claim 15, wherein said fixing is simultaneously performed for each of said semiconductor chips with said second pressure.

5. The fabrication method of the semiconductor device as claimed in claim 15, wherein said plurality of the projection electrodes are formed as studs by wire-bonding, the studs being leveled.

6. The fabrication method of the semiconductor device as claimed in claim 15, wherein said step (a) further comprises the steps of (a-1) forming a conductive adhesive on said projection electrodes.

8. The fabrication method of the semiconductor device as claimed in claim 6, wherein in the step (a-1), said conductive adhesive on the projection electrodes is formed by a conductive adhesive, that has been skidded on a plate, and then transcribed onto the projection electrodes.

15. A fabrication method of a semiconductor device comprising the steps of:

(a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;

(b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;

(c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed;

(d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and

(e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

16. A fabricating method according to claim 15, wherein in the heating step (c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate is placed.

17. A fabrication method according to claim 15, wherein in the heating step (e), heating the thermosetting insulating adhesive is performed by a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

APPEAL BRIEF FOR THE APPELLANTS

Ex parte KIRA et al.

METHOD AND SYSTEM FOR A FABRICATION SEMICONDUCTOR DEVICE

Serial Number: 08/897,953

Filed: July 24, 1997

Group Art Unit: 2814

Examiner: D. Graybill

William L. Brooks
Attorney for Appellants
Registration No. 34,129

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel (202) 659-2930
Fax (202) 887-0357

Date: July 31, 2000
Atty. Docket No. 950107A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:

KIRA, et al.

Serial Number: 08/897,953 Group Art Unit: 2814

Filed: July 24, 1997 Examiner: D. Graybill

For: METHOD AND SYSTEM FOR FABRICATING SEMICONDUCTOR DEVICE

APPEAL BRIEF

Director of Patents and Trademarks
Washington, D.C. 20231

July 31, 2000

Sir:

This is an appeal from the Office Action dated November 30, 2000 in which claims 3-6, 8 and 11-17 were finally rejected.

A Notice of Appeal and a Petition for Extension of Time were timely filed on May 30, 2000.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Fujitsu Limited
1015, Kamikodanaka, Nakahara-ku
Kawasaki-shi, Kanagawa, 211, JAPAN

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 3, 5-6, 8 and 15-17 on appeal have been finally rejected as follows:

1. Claims 3, 5-6, 8 and 15 have been finally rejected under 35 USC §103(a) as unpatentable over Appellants' Admitted Prior Art (hereinafter "**APA**") in view of JP 58180091 to Maeda (hereinafter "**Maeda**") and JP 4302444 to Koga (hereinafter "**Koga**").

2. Claims 12 and 16 have been finally rejected under 35 USC §103(a) as unpatentable over the combination of **APA**, **Maeda**, **Koga** and further in combination with U.S. Patent 5,548,091 to DiStefano (hereinafter "**DiStefano**"); and

3. Claim 17 has been finally rejected under 35 USC §103(a) as unpatentable over the combination of **APA**, **Maeda**, **Koga** and further in combination with U.S. Patent 5,115,545 to Fujimoto et al. ("**Fujimoto et al.**").

IV. STATUS OF AMENDMENTS

All amendments have been entered, including the Amendment After Final Rejection filed May 1, 2000, in which claims 4 and 11-14 were canceled and claims 5 and 6 were amended. Thus, claims 4 and 11-14 are not under consideration in this appeal, contrary to the erroneous indication by the Examiner in the Advisory Action that they are.

V. CLAIMS ON APPEAL

A clean copy of claims 3, 5-6, 8 and 15-17 on appeal is attached hereto as Exhibit A.

VI. SUMMARY OF THE INVENTION

The present invention generally relates to a fabrication method of a semiconductor device comprising the steps of: (a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips (specification, page 7, line 28 - page 8, line 11; Fig. 3, step S1); (b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate (specification, page 8, lines 23-34; Fig. 3, step S4); (c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means (Fig. 3, step S5) and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed (specification, page 8, line 35 - page 9, line 18; Fig. 3, step S6); (d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive (specification, page 9, lines 19-23; Fig. 3, step S7); and (e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips (specification, page 9, line 23 - page 10, line 13; Fig. 3, step S8).

VII. THE ISSUES

1. Whether the invention, as recited in Appellants' claims 3, 5-6, 8 and 15 on appeal are unpatentable under 35 USC §103(a) over **APA** in view of **Maeda** and **Koga**.

2. Whether the invention, as recited in Appellants' claims 12 and 16 on appeal, are unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **DiStefano**; and

3. Whether the invention, as recited in Appellants' claim 17 on appeal, is unpatentable under 35 USC §103(a) over the combination of **APA**, **Maeda**, **Koga** and **Fujimoto et al**.

VIII. GROUPING OF THE CLAIMS

Rejected claims 3, 5-6, 8 and 15-17 on appeal should stand or fall together, because claims 3, 5-6, 8 and 16-17 depend from independent claim 15.

IX. ARGUMENT WITH RESPECT TO THE ISSUES

A. THE REFERENCES

The Examiner has relied upon four (4) prior art references in the 35 USC §103(a) rejections of the claims, namely, **Maeda**, **Koga**, **DiStefano** and **Fujimoto et al**.

Maeda discloses a method of adhering leadless electrical parts in which the adhesive is heated prior to mounting of the leadless electrical parts in order to increase the viscosity of the adhesive. Then, after mounting of the leadless electrical parts on the adhesive, heat or radioactive rays are applied to the printed wiring board. Pg. 7, lines 7-21 disclose that the first heating process "is carried out from an upper place by a far-infrared-rays heater 4", as shown in Fig. 2(b).

Furthermore, pg. 7, lines 22-31 disclose that the second heating process is carried out by applying ultraviolet rays for 15 seconds by a high-pressure mercury lamp having a reflecting plate 7. Line 30 specifically refers to this heating as a "radiating process".

Kogo discloses a mounting method for a semiconductor on a substrate in which after the plurality of semiconductor elements have been bonded temporarily on the substrate via the anisotropically conductive film, the plurality of semiconductor elements are heated and pressurized collectively.

DiStefano discloses a method of mounting connection components on semiconductor chips. The method includes the step of aligning the connection component with the chip so that the leads on the connection component are aligned with contacts on the chip and bonding the bottom surface of the support structure to a surface of the chip by engaging the bottom surface of the support structure against the chip surface and activating the adhesive on the support structure bottom surface while marinating the alignment between the conductors of the connection component and the contacts on the chip. most preferably, the bonding step includes the step of moving the connection component relative to the chip in an engagement direction substantially normal to the surface of the chip after the aligning step so as to engage the bottom surface of the connection component with the surface of the chip. Such normal motion can be readily combined with an alignment process using automatic pattern recognition with other automated alignment steps without disturbing the alignment achieved by these steps.

The bonding step desirably includes the step of momentarily heating the adhesive while the adhesive is engaged between the bottom surface of the connection component and the surface of th chip. In a particularly preferred arrangement, the chip may be at an elevated temperature prior to

the bonding step, so that the adhesive is heated by heat transferred from the chip to the adhesive when the adhesive is engaged with the chip surface. The adhesive desirably is solid and non-tacky prior to engagement with the hot chip.

Fujimoto discloses an apparatus for connecting a semiconductor device having multi-electrodes at small pitches to a wiring board in such a manner so as to secure the alignment between the electrodes and he wiring patterns, the chips being secured to the wiring board with an insulating resin of a photo-setting nature. The apparatus eliminates the necessity of using heat or supersonic waves, thereby reducing equipment costs.

B. SUMMARY OF EXAMINER'S REJECTIONS

1. Claims 3, 5-6, 8 and 15 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over th combination of **APA** and **Maeda** and further in combination with **Koga**.

The Examiner urges that Appellants teach as conventional a process comprising the steps of forming leveled projection electrode studs 14 on a semiconductor chip 11 by wire-bonding; forming conductive adhesive 16a on the electrodes by a conductive adhesive 16 that has been skidded on a plate 15a and then transcribed onto the electrodes; applying a thermosetting insulating adhesive 18 to areas of mounting parts where the chip is to be mounted on a substrate 17; aligning the chip to the mounting parts at a first stage and performing a first fixing of the chips with a first pressure by a bonding head to which the chip is absorbed; and, thereafter, heating the substrate on which the chip is fixed with a thermosetting temperature of the adhesive. See page 1, line 23 to page 2, line 22 of the specification of the application on appeal.

The Examiner asserts, however, that Appellants do not appear to explicitly teach as conventional a process comprising a plurality of chips, and the steps of heating the adhesive on the substrate with a half-thermosetting temperature os as to harden the adhesive on the substrate to a half-thermosetting state by heating means; moving the substrate to a second stage, while the chips on the substrate are held at their position by the half-thermosetting state of the adhesive; thereafter, heating at the second stage the substrate on which the chips are fixed. The Examiner cited **Maeda** for teaching this process at page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full paragraph. Moreover, the Examiner urges that it would have been obvious to combine the process of **Maeda** with the process of **APA** because it would enable accurate alignment of plural chips before the final fixing step of the conventional art.

The Examiner urges that the combination of **APA** and **Maeda** does not appear to explicitly teach a process comprising wherein a second fixing is simultaneously performed for each of the chips with a second pressure, and wherein in the heating step (e) while heating the adhesive on the mounting parts a pressure is applied to the chips. Nevertheless, the Examiner cited **Kogo** for teaching a process comprising wherein a second fixing is simultaneously performed for each of plural chips with second pressure, and wherein in a heating step while heating an adhesive on mounting parts a pressure is applied to the chips. The Examiner concludes that it would have been obvious to combine the process of **Koga** with the process of the applied prior art because it would facilitate bonding.

The Examiner admits that the combination of applied prior art does not appear to explicitly teach a process wherein the second pressure is greater than the first pressure, but urges that it would

have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure limitation, and urges that it appears *prima facie* that the process would possess utility using another relative pressure. The Examiner notes that it has been held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

2. Claims 12 and 16 on appeal were finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga**, as applied to claims 3, 5-6, 8 and 15, and further in combination with **DiStefano**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising wherein in the heating step (c) heating the adhesive is performed by a heat plate on which the substrate is placed. Regardless, the Examiner urges that, at column 9, lines 3-63 **DiStefano** teaches a process comprising wherein in a heating step heating the adhesive is performed by a heat plate 58 on which a substrate mounting chips is placed. The Examiner urges that it would have been obvious to combine the process of **DiStefano** with the process of the applied prior art because it would facilitate adhesive curing.

3. Claim 17 on appeal was finally rejected under 35 USC §103(a) as being unpatentable over the combination of **APA**, **Maeda** and **Koga** as applied to claims 3, 5-6, 8 and 15 supra, and further in combination with **Fujimoto**.

The Examiner admits that the combination of **APA**, **Maeda** and **Koga** does not appear to explicitly teach a process comprising a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate. The

Examiner cites **Koga** for teaching a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is provided on the heat block corresponding to the mounting parts of the substrate. The Examiner cites **Fujimoto** for teaching a single bonding head 52 for each chip. The Examiner urges that it would have been obvious to combine the process of **Fujimoto** and the process of **Koga** by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. The Examiner urges that it would have been obvious to combine the heat block of the combination of **Fujimoto** and **Koga** with **APA** because it would facilitate bonding.

C. APPELLANTS' ARGUMENT

1. APA, IN COMBINATION WITH MAEDA AND KOGA, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 3, 5-6, 8 AND 15 ON APPEAL.

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that the structural elements by combined in a similar manner as the claimed invention. See, e.g., *Panduit*

Corp. v. Dennison Mfg. Co., 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), vacated on other grounds, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

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Summarizing, **Maeda** teaches the step of heating an insulating adhesive to increase the viscosity thereof so as to prevent electrical parts from moving. However, **Maeda** fails to teach or suggest that the electrical parts are held with pressure, as recited in the claims on appeal.

The Examiner has urged, however, that application of such pressure would be inherent in **Maeda** because **Maeda** teaches the use of a bonding head to mount the chips into the adhesive. Column 3, lines 3-5 disclose "loading the electronic parts on the printed circuit substrate and pressing them on the adhesive."

Maeda fails to teach, mention or suggest a second pressure application of pressure on the chips which is greater than the first application of pressure, as recited in the claims on appeal.

The Examiner has applied **Koga** for teaching two separate application steps, as noted in the Abstract of **Koga**:

> ... Then, since the surface of the anisotropically conductive film 7 is provided with adhesive power, the semiconductor element 1 is bonded temporarily to a substrate 5. The substrate 5 which has finished its temporarily bonding process is conveyed to a bonding sage 11 by using a substrate conveyance device 12: it is position (sic). A bonding head 25 is driven downward in a state that the temperature at its lower-end part is kept at 190°C; it presses many semiconductor elements (sic), ... in the direction of the substrate 5 at a definite pressure.

Koga fails to explicitly teach, however, that the second pressure is greater than the first pressure, as recited in the claims on appeal, as the Examiner has admitted. The Examiner has urged, however, that this would be an obvious choice ascertainable by routine experimentation. The Examiner has held that optimization of range limitations are *prima facie* obvious absent a disclosure that the limitations are for a "particular unobvious purpose, produce an unexpected result, or otherwise critical."

Appellants respectfully disagree and submit that such a claimed relation between the first and second pressure would require undue experimentation to produce. **Koga** fails to provide any reason why such relationship would be important.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

2. APA, IN COMBINATION WITH MAEDA, KOGA AND DISTEFANO, FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIMS 12 AND 16 ON APPEAL.

DiStefano has been cited for teaching a heating step performed by a heat plate 58 on which a substrate is placed.

DiStefano is not combinable with **Maeda** to teach the present invention because, while **DiStefano** discloses conductive heating, which requires pressure, **Maeda** specifically discloses radiative heating without pressure.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

3. APA, IN COMBINATION WITH MAEDA, KOGA AND FUJIMOTO ET AL., FAILS TO TEACH THE METHOD STEPS AS RECITED IN CLAIM 17.

Fujimoto et al. has been cited for teaching a single bonding head 52 for each chip "without the need for using heat or supersonic waves" (see Abstract of **Fujimoto et al.**"), which teaches away from the two heating steps recited in claim 15 on appeal, from which claim 17 on appeal depends.

DiStefano and **Fujimoto et al.** both fail to teach, mention, or suggest the two-step heating with pressure applied to the semiconductor chips as recited in claim 15 on appeal and none of the cited references teaches, mentions, or suggests the relationship between the pressure applied in the two heating steps, as recited in claim 15 on appeal.

Thus, the §103(a) rejection is erroneous and should be withdrawn.

X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's 35 USC §103(a) rejections of claims 3, 5-6, 8 and 15-17 on appeal and to instruct the Examiner to pass this application to issue.

In the event this paper is not timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI
McLELAND & NAUGHTON

William L. Brooks
Attorney for Applicants
Registration No. 34,129

Attorney Docket No. 950107A
1725 K Street, N.W.
Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
WLB:mlg
Enclosure: Appendix A containing Claims on Appeal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:

KIRA, et al.

Serial Number: 08/897,953 Group Art Unit: 2814

Filed: July 24, 1997 Examiner: D. Graybill

For: METHOD AND SYSTEM FOR FABRICATING SEMICONDUCTOR DEVICE

CLAIMS ON APPEAL

Director of Patents and Trademarks
Washington, D.C. 20231 July 31, 2000

Sir:

The claims on appeal are 3, 5-6, 8 and 15-17, presented below.

3. The fabrication method of the semiconductor device as claimed in claim 15, wherein said fixing is simultaneously performed for each of said semiconductor chips with said second pressure.

5. The fabrication method of the semiconductor device as claimed in claim 15, wherein said plurality of the projection electrodes are formed as studs by wire-bonding, the studs being leveled.

6. The fabrication method of the semiconductor device as claimed in claim 15, wherein said step (a) further comprises the steps of (a-1) forming a conductive adhesive on said projection electrodes.

8. The fabrication method of the semiconductor device as claimed in claim 6, wherein in the step (a-1), said conductive adhesive on the projection electrodes is formed by a conductive adhesive, that has been skidded on a plate, and then transcribed onto the projection electrodes.

15. A fabrication method of a semiconductor device comprising the steps of:

(a) forming a plurality of projection electrodes on each of a plurality of semiconductor chips;

(b) applying a thermosetting insulating adhesive to areas of mounting parts where the semiconductor chips are to be mounted on a substrate;

(c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means and, then, aligning the semiconductor chips to the mounting parts of the substrate at a first stage and performing a first fixing of the semiconductor chips with a first pressure by a bonding head to which the semiconductor chips are absorbed;

(d) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and

(e) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips with a second pressure, wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

16. A fabricating method according to claim 15, wherein in the heating step (c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate is placed.

17. A fabrication method according to claim 15, wherein in the heating step (e), heating the thermosetting insulating adhesive is performed by a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.